μPD7500x/75P008
General-Purpose 4-Bit Microcomputers With Multiple I/Os

Description

The μPD7500x/75P008 is a family of single-chip CMOS microcomputers containing CPU, ROM, RAM, I/O ports, several timer/counters, vectored interrupts, subsystem clock, and serial interface.

The instruction set allows the user to manipulate RAM data and I/O ports in 1-, 4-, and 8-bit units. The devices are ideally suited for controlling VCRs, telephones, and meters.

Both EPROM and OTP versions are available. See ordering information.

Features

- 103 instructions
  - Bit manipulation
  - 4-bit and 8-bit transfer
  - 1-byte relative branch
  - GETI instruction, to convert one 2-byte or two 1-byte instructions into a single 1-byte instruction
- Fast execution time (@ 4.19 MHz)
  - High-speed cycle: 0.95 μs
  - Lower-voltage cycles: 1.91 and 15.3 μs
- Program ROM
  - μPD75004: 4096 bytes
  - μPD75006: 6016 bytes
  - μPD75008/P008: 8064 bytes
- 512 x 4 bits of RAM
  - Allows operation on 1, 4, or 8 bits
- Bit sequential buffer
  - 16-bit, bit manipulation memory
- Eight 4-bit registers
- Accumulators
  - 1-bit (CY)
  - 4-bit (A)
  - 8-bit (XA)
- 26 I/O lines
  - 8 N-channel open drain; can withstand 10 V
  - 18 outputs directly drive LEDs (I_{sink} = 15 mA rms)
- One external event input
- Three timers
  - 8-bit basic interval timer
  - 8-bit timer/event counter
  - 14-bit watch timer
- 8-bit serial interface
  - SBI mode
  - 2- or 3-wire mode: data transfer can be full duplex or receive only, and can be MSB or LSB first
- Vectored interrupts
  - Three external interrupts
  - Three internal interrupts
  - Nine inputs which each generate one interrupt request
- Eight input-only lines
- Standby modes
  - HALT mode: stops CPU only
  - STOP mode: stops main system clock
- Mask option pull-up resistors for ports 4 and 5
- Operates with oscillator or ceramic resonator
- CMOS operation with V_{DD} from 2.7 to 6.0 V
- Power consumption @ 5 V and 4.19 MHz
  - Normal mode: 2.5 mA typical
  - HALT mode: 0.5 mA typical
  - STOP mode: 0.5 μA typical
- Programmable version:
  - μPD75P008 OTP

Ordering Information

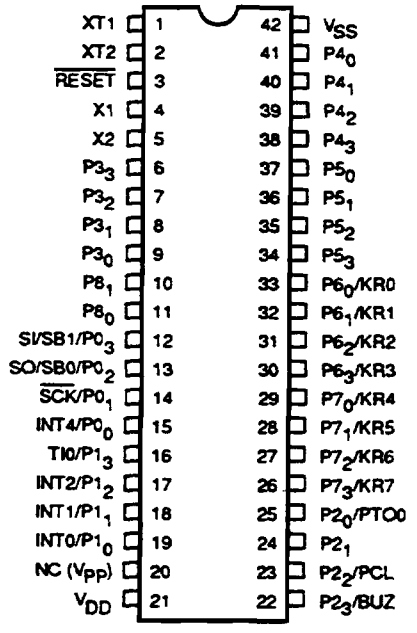
Part Number	Package Type	ROM
μPD75004CU-xxx	42-pin plastic SDIP	Mask ROM
μPD75004GB-xxx-3B4	44-pin plastic QFP	Mask ROM
μPD75006CU-xxx	42-pin plastic SDIP	Mask ROM
μPD75006GB-xxx-3B4	44-pin plastic QFP	Mask ROM
μPD75008CU-xxx	42-pin plastic SDIP	Mask ROM
μPD75008GB-xxx-3B4	44-pin plastic QFP	Mask ROM
μPD75P008CU	42-pin plastic SDIP	OTP
μPD75P008GB-3B4	44-pin plastic QFP	OTP

Notes:

(1) xxx indicates ROM code suffix

Pin Configurations

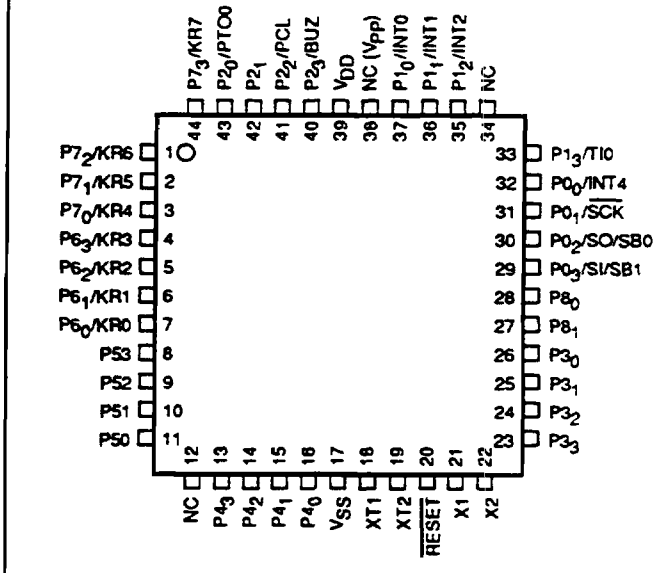
42-Pin Plastic SDIP



Note : V_{PP} is the programming pin in the 75P008 and should be connected to V_{DD}. It is not connected in the mask ROM ports.

83RD-6363A

44-Pin Plastic QFP



Note : V_{PP} is the programming pin in the 75P008 and should be connected to V_{DD}. It is not connected in the mask ROM ports.

83RD-6364A

Pin Identification

Symbol	Function
NC (V_{PP})	No connection (programming voltage for μPD75P008
$P0_0$/INT4	Port 0 input; interrupt 4
$P0_1$/$\overline{SCK}$	Port 0 input; serial clock
$P0_2$/SO/SB0	Port 0 input; serial out; serial interface
$P0_3$/SI/SB1	Port 0 input; serial in; serial interface
$P1_0$/INT0	Port 1 input; interrupt 0
$P1_1$/INT1	Port 1 input; interrupt 1
$P1_2$/INT2	Port 1 input; interrupt 2
$P1_3$/TI0	Port 1 input; timer 0 input
$P2_0$/PTO0	Port 2 I/O; timer/event counter output
$P2_1$	Port 2 I/O
$P2_2$/PCL	Port 2 I/O; clock output
$P2_3$/BUZ	Port 2 I/O; buzzer output
$P3_0$-$P3_3$	Port 3 I/O
$P4_0$-$P4_3$	Port 4 I/O
$P5_0$-$P5_3$	Port 5 I/O
$P6_0$/KR0	Port 6 I/O; key scan input 0
$P6_1$/KR1	Port 6 I/O; key scan input 1
$P6_2$/KR2	Port 6 I/O; key scan input 2
$P6_3$/KR3	Port 6 I/O; key scan input 3
$P7_0$/KR4	Port 7 I/O; key scan input 4
$P7_1$/KR5	Port 7 I/O; key scan input 5
$P7_2$/KR6	Port 7 I/O; key scan input 6
$P7_3$/KR7	Port 7 I/O; key scan input 7
$P8_0$-$P8_1$	Port 8 I/O
$\overline{RESET}$	Reset input
V_{DD}	Positive power supply
V_{SS}	Ground
X1, X2	Main clock inputs
XT1, XT2	Subsystem clock inputs

PIN FUNCTIONS

$P0_0$-$P0_3$, INT4, $\overline{SCK}$, SO/SB0, SI/SB1 (Port 0, Interrupt 4, Serial Interface)

These pins can be used as 4-bit input port 0. $P0_0$ can also be used for vectored interrupt 4, which interrupts on either the leading edge or the trailing edge of the signal. $P0_1$-$P0_3$ may also be used for the serial interface in the SBI, 2-wire or 3-wire mode. SI is the serial input, SO is the serial output, and $\overline{SCK}$ is the serial clock. Reset causes these pins to default to the port 0 input mode.

$P1_0$-$P1_3$, INT0-INT2, TI0 (Port 1, Edge-Triggered Interrupts, Timer Input)

These pins can be used as 4-bit input port 1. $P1_0$ and $P1_1$ can also be used for edge-triggered interrupts INT0 and INT1. $P1_2$ can be used for INT2, which is also an edge-triggered input, but one which generates an interrupt request and does not cause an interrupt. $P1_3$ can be used as an input clock to the timer/event counter to count external events. Reset causes these pins to default to the port 1 input mode.

$P2_0$-$P2_3$, PTO_0, PCL, BUZ (Port 2, Timer/Event Counter, Clock, or Buzzer Output)

These pins can be used as 4-bit I/O port 2. When used as an output the data is latched. When used as an input port the port outputs are three-state. $P2_0$ can also be used as the output of the timer/event counter flip flop (TOUT); $P2_2$ can be used as the output for the clock generator (PCL); and $P2_3$ can be used to output square waves for a buzzer. Reset causes these pins to default to the port 2 input mode.

$P3_0$-$P3_3$ (Port 3)

These pins are used for I/O port 3. Each bit in this port can be independently programmed to be either an input or an output. This port has latched outputs, and can directly drive LEDs. A reset signal causes this port to default to the input mode.

$P4_0$-$P4_3$, $P5_0$-$P5_3$ (Ports 4 and 5)

Port 4 and 5 are 4-bit I/O ports which can be combined together to function as a single 8-bit port. They have latched outputs. Port 4 will directly drive LEDs. Outputs are N-channel open drain, and can withstand up to 10 volts; pull-up resistor mask options are available for these ports. A reset signal causes these ports to default to the input mode.

$P6_0$-$P6_3$, $P7_0$-$P7_3$, KR0-KR7 (Ports 6, 7, and Edge Detection)

Ports 6 and 7 are 4-bit I/O ports with latched outputs. Each pin of port 6 can be independently programmed to be either an input or an output, while port 7 can be programmed to be either all inputs or all outputs. Ports 6 and 7 can be paired together to function as one 8-bit port. Alternately, these pins may be used to detect the falling edge of inputs KR0-KR3 (port 6) and KR4-KR7 (port 7). A reset signal causes these ports to default to the input mode.

$P8_0$-$P8_1$ (Port 8)

Port 8 is a 2-bit I/O port. Outputs are latched. A reset signal causes this port to default to the input mode.

NC/V_{PP} (No Connection/Programming Pin)

This pin may be left unconnected when using the μPD7500x. When using the programmable devices, this pin is used to input the programming voltage during the EPROM write/verify cycles. During normal operation of the programmable device, this pin should be tied to V_{DD}.

X1, X2 (Main System Clock Inputs)

These pins are the main system clock inputs. The clock can be either a ceramic resonator or a crystal; an external logic signal may also be used.

XT1, XT2 (Subsystem Clock Inputs)

These pins are the subsystem clock inputs. The clock can be either a ceramic resonator or a crystal; an external logic signal may also be used.

$\overline{RESET}$ (Reset)

This is the reset input, and it is active low.

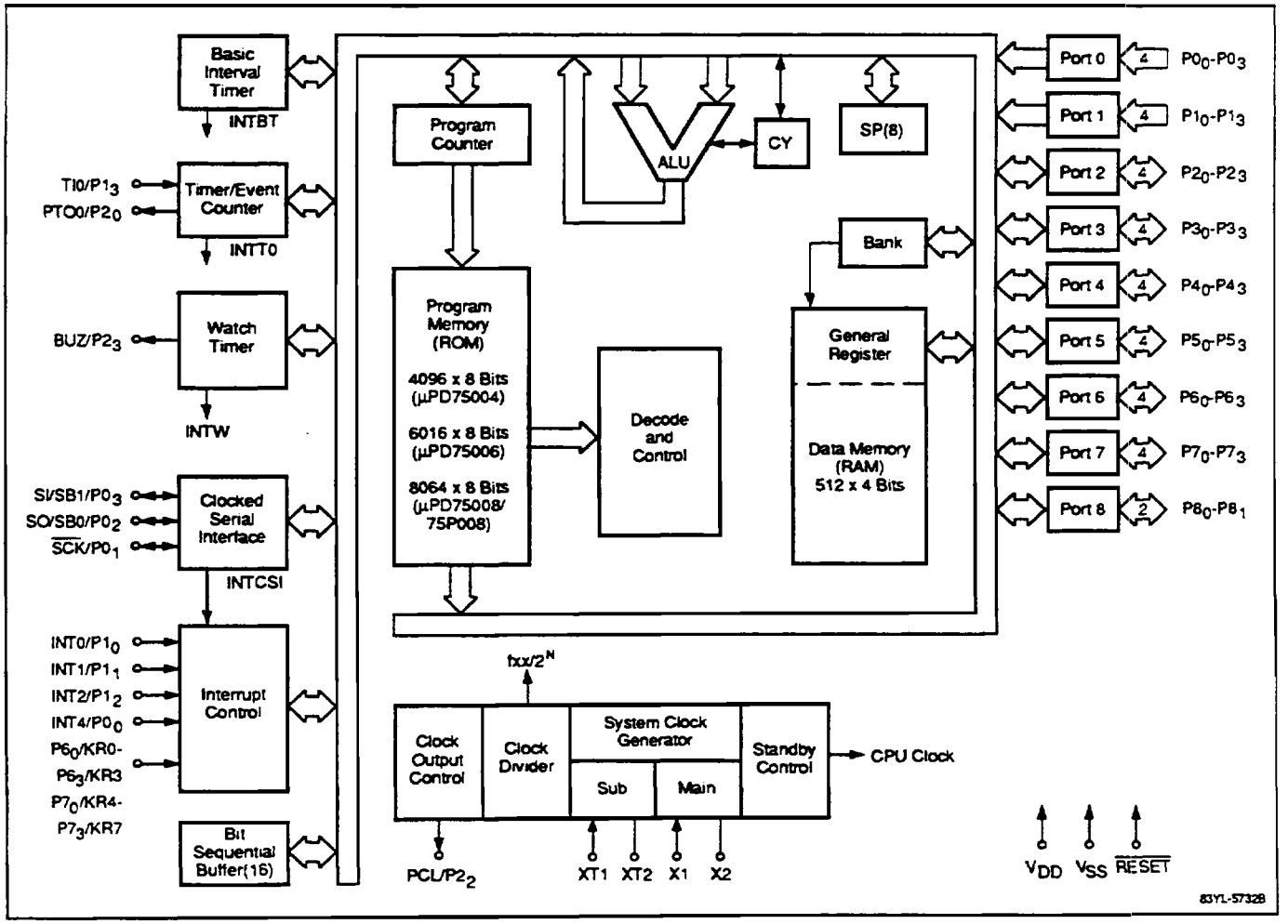
V_{DD} (Power Supply)

The system positive power supply pin.

V_{SS} (Ground)

System ground.

Block Diagram



Product Comparison

Item	μPD75004	μPD75006	μPD75008	μPD75P008CU/GB
Program memory	Mask ROM 000H–FFFH 4096 x 8 bits	Mask ROM 0000H–177FH 6016 x 8 bits	Mask ROM 0000H–1F7FH 8064 x 8 bits	OTP 0000H–1F7FH 8064 x 8 bits
Data memory	512 x 4 bits Bank 0: 256 x 4 Bank 1: 256 x 4	512 x 4 bits Bank 0: 256 x 4 Bank 1: 256 x 4	512 x 4 bits Bank 0: 256 x 4 Bank 1: 256 x 4	512 x 4 bits Bank 0: 256 x 4 Bank 1: 256 x 4
3-byte branch instruction	None	Provided	Provided	Provided
Other instructions	Provided	Provided	Provided	Provided
Program counter	12 bits	13 bits	13 bits	13 bits
Pull-up resistor, ports 0–3; 6–8	Can be specified by software			
Pull-up resistor, ports 4, 5	Mask option	Mask option	Mask option	Not provided
Operating voltage range	2.7 to 6.0 V	2.7 to 6.0 V	2.7 to 6.0 V	5 V ± 5%
Package	42-pin plastic shrink DIP 44-pin plastic QFP (bent)			42-pin plastic shrink DIP 44-pin plastic QFP (bent)

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

T_A = 25°C

Supply voltage, V_{DD}	−0.3 to +7.0 V
Programming voltage, V_{PP} (μPD75P008 only)	−0.3 to +13.5 V
Input voltage, V_{IN1}	−0.3 to V_{DD} + 0.3 V
Input voltage, V_{IN2} (Ports 4 and 5 with open drain)	−0.3 to 11 V
Output voltage, V_O	−0.3 to V_{DD} + 0.3 V
High-level output current, I_{OH}	
Single pins	−10 mA
All pins	−30 mA
Low-level output current, I_{OL} (Note 1)	
Ports 0, 3-5 (one port pin)	30 mA peak, 15 mA rms
All ports except 0, 3-5	20 mA peak, 10 mA rms
Total of ports 0, 3-5, 8	160 mA peak, 120 mA rms
Total of ports 2, 6, 7	66 mA peak, 33 mA rms
Storage temperature, T_{STG}	−65 to +150°C
Operating temperature, T_{OPT} (μPD7500x)	−40 to +85°C
Operating temperature, T_{OPT} (μPD75P008 only)	−10 to +70°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage.

Notes:

(1) Effective value = Peak value x $(Duty)^{1/2}$

Capacitance

T_A = 25°C; V_{DD} = 0 V

Parameter	Symbol	Min	Max	Unit	Conditions
Input capacitance	C_{IN}		15	pF	f = 1 MHz; all unmeasured pins returned to ground
Output capacitance	C_{OUT}		15	pF	
I/O capacitance	C_{IO}		15	pF	

Main System Clock Oscillator Characteristics

μPD7500x: T_A = −40 to +85°C, V_{DD} = 2.7 to 6.0 V
μPD75P008: T_A = −10 to +70°C, V_{DD} = 4.5 to 5.5 V

Oscillator	Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Ceramic resonator (Figure 1A)	Oscillation frequency (Note 1)	f_{XX}	1.0		5.0	MHz	After V_{DD} reaches the minimum oscillator operating voltage range.
	Oscillation stabilization time (Note 2)				4 (Note 3)	ms	
Crystal resonator (Figure 1A)	Oscillation frequency (Note 1)	f_{XX}	1.0	4.19	5.0	MHz	
	Oscillation stabilization time (Note 2)				10 (Notes 3, 4)	ms	
					30 (Notes 3, 5)	ms	
External clock (Figure 1B)	X1 input frequency (Note 1)	f_{XX}	1.0		5.0	MHz	
	X1 input low- and high-level width	t_{XH}, t_{XL}	100		500	ns	

Notes:

(1) The oscillation frequency and X1 input frequency are included only to show the characteristics of the oscillators. Refer to the AC Characteristics table for actual instruction execution times.

(2) The oscillation stabilization time is the time required for the oscillator to stabilize after voltage is applied or the STOP mode is released.

(3) Values shown are for the recommended resonators. Values for resonators not shown in this data sheet should be obtained from the manufacturer's specification sheets.

(4) V_{DD} = 4.5 to 6.0 V for 7500x or 4.5 to 5.5 V for μPD75P008.

(5) For μPD7500x only at V_{DD} = 2.7 – 6.0 V

Subsystem Clock Oscillator Characteristics

μPD7500x: T_A = −40 to +85°C; V_{DD} = 2.7 to 6.0 V
μPD75P008: T_A = −10 to +70°C; V_{DD} = 4.5 to 5.5 V

Oscillator	Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Crystal resonator (Figure 2A)	Oscillation frequency	f_{XT}	32	32.768	35	kHz	
	Oscillation stabilization time			1.0	2	s	See note 4 under Main System Oscillator Characteristics
					2	s	See note 5 under Main System Oscillator Characteristics
External clock (Figure 2B)	XT1 input frequency	f_{XT}	32		100	kHz	
	XT1 input low- and high-level width	t_{XTH}, t_{XTL}	5		15	μs	

Recommended Oscillator Circuit Constants (For 7500x only)

Main system clock = Ceramic; T_A = −40 to +85°C

Manufacturer	Part Number (Note 1)	Frequency (MHz)	C1 (pF)	C2 (pF)	Oscillation Voltage	
					Min (V)	Max (V)
Murata	CSA x.xxMK	1.0–1.99	30	30	2.7	6.0
	CSA x.xxMG093	2.0–2.44	30	30	2.7	6.0
	CST x.xxMG093	2.0–2.44	(Note 2)	(Note 2)	2.7	6.0
	CSA x.xxMGU	2.45–5.0	30	30	2.7	6.0
	CST x.xxMGU	2.45–5.0	(Note 2)	(Note 2)	2.7	6.0
	CSA x.xxMG	2.0–5.0	30	30	3.0	6.0
	CST x.xxMG	2.0–5.0	(Note 2)	(Note 2)	3.0	6.0
Kyocera	KBR 1000H	1.0	100	100	2.7	6.0
	KBR 2.0MS	2.0	47	47	2.7	6.0
	KBR 4.0MS	4.0	33	33	2.7	6.0
	KBR 5.0M	5.0	33	33	3.0	6.0

Notes:

(1) x.xx indicates frequency.

(2) C1 and C2 not required; they are in the oscillator.

Figure 1. Main System Clock Configurations

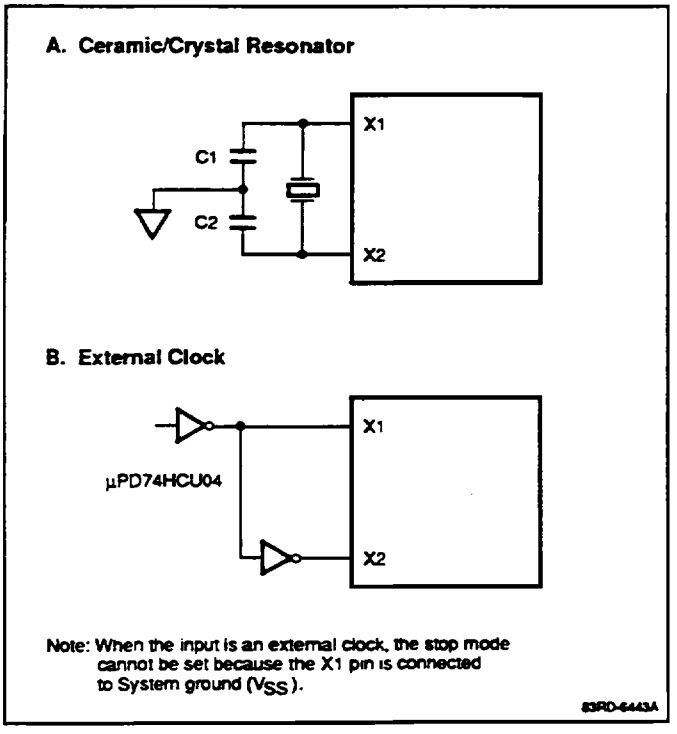
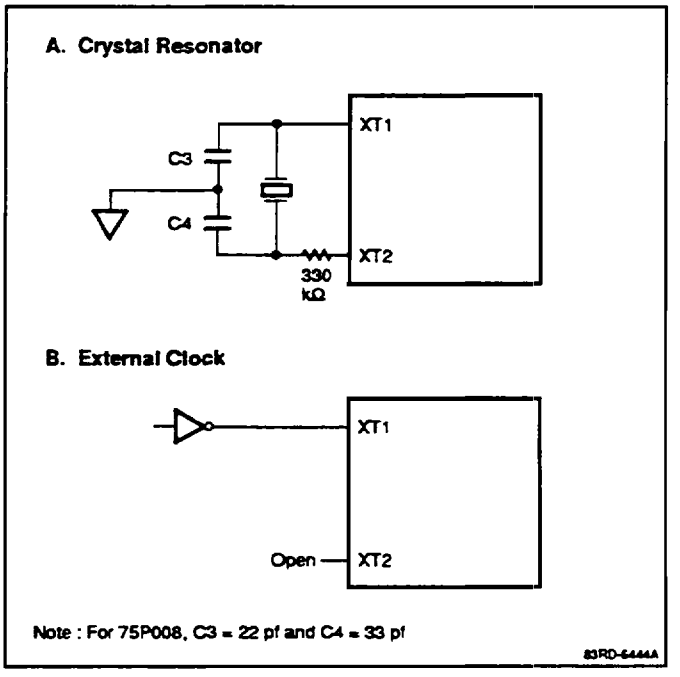


Figure 2. Subsystem Clock Configurations



Recommended Oscillator Circuit Constants (For 7500x only)

Main system clock = Crystal; T_A = −20 to +70°C

Manufacturer	Part Number	Frequency (MHz)	C1 (Note 1) (pF)	C2 (pF)	Oscillation Voltage	
					Min (V)	Max (V)
Kinseki	HC-6U	1.0–2.0	20	22	2.7	6.0
	HC-18U, HC-43/U, HC-49/U	2.0–5.0	20	22	2.7	6.0

Notes:

(1) Keep C1 between 15 and 33 pF when adjusting the oscillation frequency.

Recommended Oscillator Circuit Constants (For 7500x only)

Subsystem clock = Crystal; T_A = −10 to +60°C

Manufacturer	Part Number	Frequency (MHz)	C3 (Note 1) (pF)	C4 (pF)	Oscillation Voltage	
					Min (V)	Max (V)
Kinseki	P-3	32.768	18	18	2.7	6.0

Notes:

(1) Keep C3 between 10 and 33 pF when adjusting the oscillation frequency.

DC Characteristics

μPD7500x: T_A = −40 to +85°C, V_{DD} = 2.7 to 6.0 V
μPD75P008: T_A = −10 to +70°C, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
High-level input voltage	V_{IH1}	$0.7V_{DD}$		V_{DD}	V	Ports 2, 3, 8
	V_{IH2}	$0.8V_{DD}$		V_{DD}	V	Ports 0, 1, 6, 7, and $\overline{RESET}$
	V_{IH3}	$0.7V_{DD}$		V_{DD}	V	Ports 4 and 5; built-in pull-up resistor
		$0.7V_{DD}$		10	V	Ports 4 and 5 with open drain
	V_{IH4}	V_{DD}−0.5		V_{DD}	V	X1, X2, XT1
Low-level input voltage	V_{IL1}	0		$0.3V_{DD}$	V	Ports 2, 3, 4, 5, 8
	V_{IL2}	0		$0.2V_{DD}$	V	Ports 0, 1, 6, 7; $\overline{RESET}$
	V_{IL3}	0		0.4	V	X1, X2, XT1
High-level output voltage	V_{OH1} (Note 1)	V_{DD}−1.0			V	Ports 0, 2, 3, 6, 7, 8; I_{OH} = −1 mA
	V_{OH2} (Note 2)	V_{DD}−0.5			V	Ports 0, 2, 3, 6, 7, 8; V_{DD} = 2.7 to 6.0 V; I_{OH} = −100 μA
Low-level output voltage	V_{OL1}		0.4	2.0	V	Ports 4 and 5; (Note 1); I_{OL} = 15 mA;
			0.6	2.0	V	Port 3; (Note 1); I_{OL} = 15 mA
				0.4	V	Ports 0, 2-8; (Note 1); I_{OL} = 1.6 mA
				0.5 (Note 2)	V	Ports 0, 2-8; V_{DD} = 4.5 to 6.0 V; I_{OL} = 400 μA
	V_{OL2}			$0.2V_{DD}$ (Note 1)	V	SB0, 1 open drain; pull-up resistance ≥ 1kΩ
				$0.2V_{DD}$ (Note 2)	V	SB0, 1 open drain; V_{DD} = 2.7 to 6.0 V; pull-up resistance ≥ 5kΩ
High-level input leakage current	I_{LIH1}			3	μA	All except X1, X2, and XT1; V_{IN} = V_{DD}
	I_{LIH2}			20	μA	X1, X2, and XT1; V_{IN} = V_{DD}
	I_{LIH3}			20	μA	Ports 4, 5 with open drain; V_{IN} = 10 V

DC Characteristics (cont)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Low-level input leakage current	I_{LIL1}			-3	μA	All except X1, X2, and XT1; V_{IN} = 0 V
	I_{LIL2}			-20	μA	X1, X2, and XT1; V_{IN} = 0 V
High-level output leakage current	I_{LOH1}			3	μA	All except ports 4 and 5 with open drain; $V_{OUT} = V_{DD}$
	I_{LOH2}			20	μA	Ports 4 and 5 with open drain; V_{OUT} = 10 V
Low-level output leakage current	I_{LOL}			-3	μA	V_{OUT} = 0 V
Built-in pull-up resistor	R_{L1}	15	40	80	kΩ	Ports 0-3, 6-8 (except $P0_0$); V_{IN} = 0 V; V_{DD} = 5.0 V ± 10%
		30 (Note 2)		300 (Note 2)	kΩ	Ports 0-3, 6-8 (except $P0_0$); V_{IN} = 0 V; V_{DD} = 3.0 V ± 10%
	R_{L2} (Note 2)	15	40	70	kΩ	Ports 4, 5; $V_{OUT} = V_{DD}$ -2.0 V; V_{DD} = 5.0 V ± 10%
		10		60	kΩ	Ports 4, 5; $V_{OUT} = V_{DD}$ -2.0 V; V_{DD} = 3.0 V ± 10%
Supply current (Note 3)	I_{DD1}	(Note 2)	2.5	8.0	mA	V_{DD} = 5.0 V ± 10% (Notes 4, 6)
		(Note 2)	0.35	1.2	mA	V_{DD} = 3.0 V ± 10% (Notes 4, 7)
		(Note 8)	5	15	mA	V_{DD} = 5 V ±10%; (Notes 4, 6)
	I_{DD2}		500	1500	μA	HALT mode; V_{DD} = 5 V ± 10% (Note 4)
		(Note 2)	150	450	μA	HALT mode; V_{DD} = 3 V ± 10%
	I_{DD3}	(Notes 2, 5)	30	90	μA	V_{DD} = 3 V ± 10%
		(Notes 5, 8)	350	1000	μA	V_{DD} = 5 V ±10%
	I_{DD4}	(Notes 2, 5)	5	15	μA	HALT mode; V_{DD} = 3 V ± 10%
		(Notes 5, 8)	35	100	μA	HALT mode V_{DD} = 5 V ±10%
	I_{DD5}		0.5	20	μA	STOP mode; XT1 = 0 V; V_{DD} = 5.0 V ± 10%
		(Note 2)	0.1	10	μA	STOP mode; XT1 = 0 V; V_{DD} = 3.0 V ± 10%
		(Note 2)	0.1	5	μA	STOP mode; XT1 = 0 V; V_{DD} = 3.0 V ± 10%; T_A = 25°C

Notes:

(1) V_{DD} = 4.5 to 6.0 V for 7500x and V_{DD} = 4.5 to 5.5 V for 75P008.

(2) For 7500x only.

(3) Does not include pull-up resistor current.

(4) 4.19 MHz crystal oscillator; C1 = C2 = 22 pF.

(5) 32.768 kHz crystal oscillator.

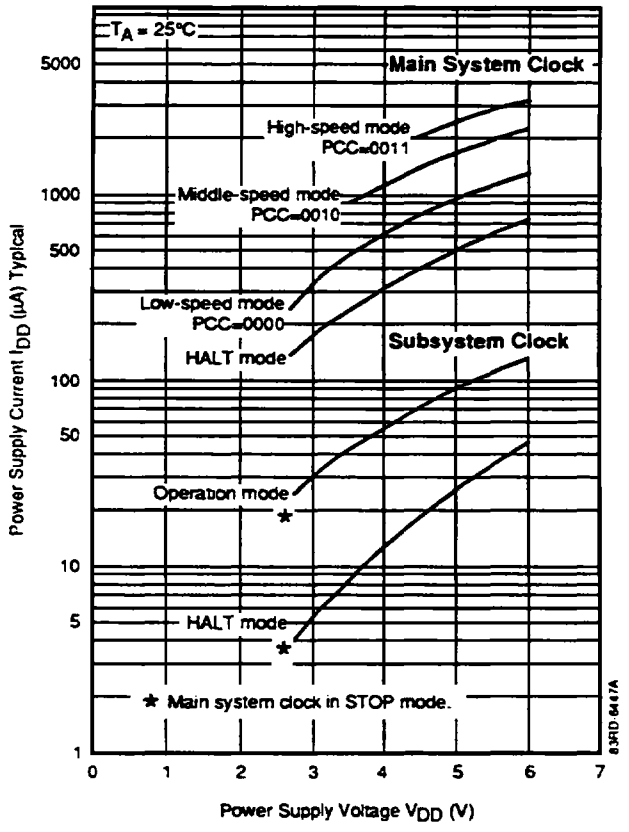
(6) When operated in the high-speed mode with the processor clock control register (PCC) set to 0011.

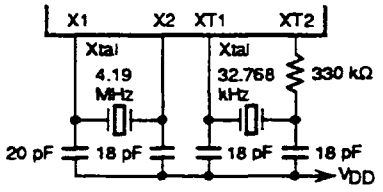
(7) When operated in the low-speed mode with the PCC set to 0000.

(8) For 75P008 only.

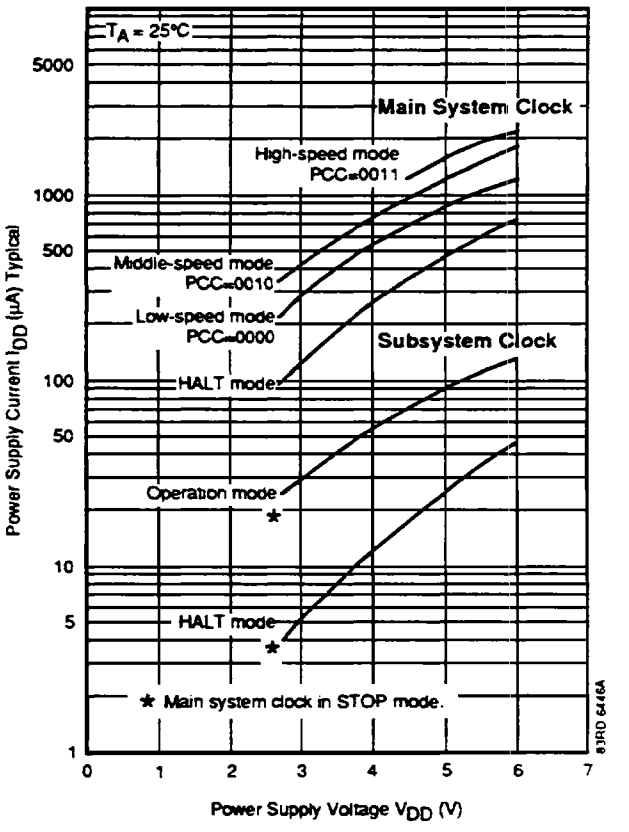
DC Characteristics

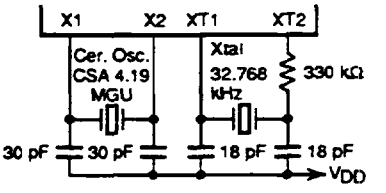
I_{DD} vs V_{DD} (Crystal Oscillator at 4.19 MHz)





I_{DD} vs V_{DD} (Ceramic Oscillator at 4.19 MHz)

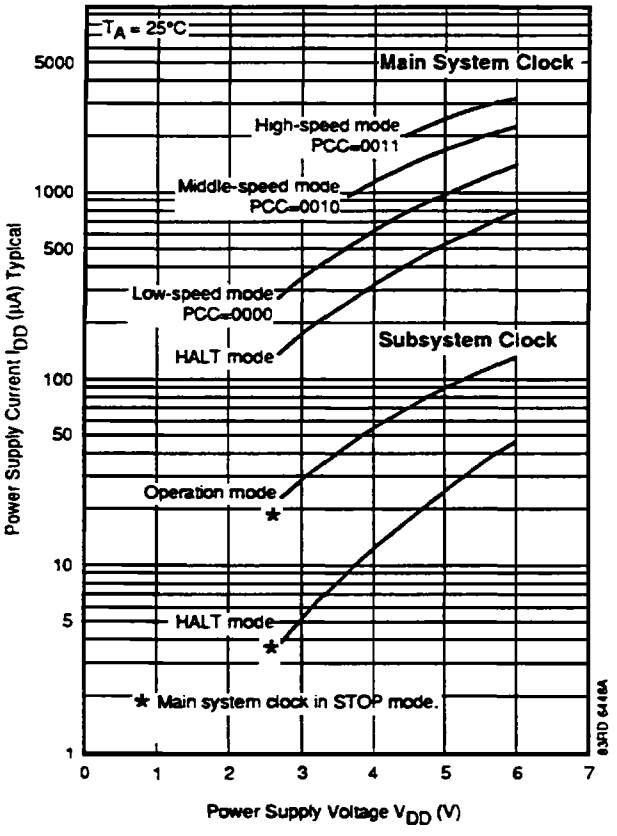




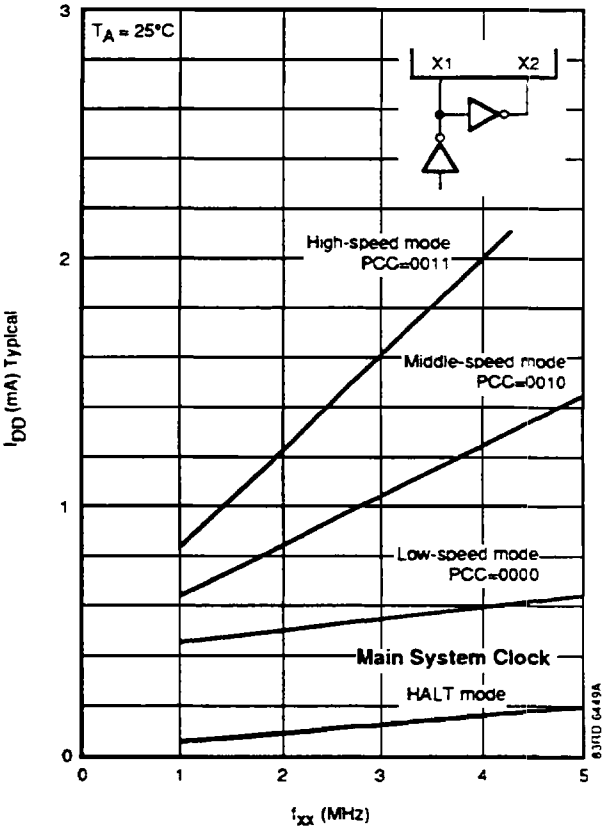
Note: Values of I_{DD} are about 10% larger using a ceramic oscillator as compared to a crystal oscillator.

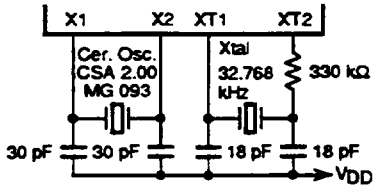
DC Characteristics (cont)

I_{DD} vs V_{DD} (Ceramic Oscillator at 2.00 MHz)

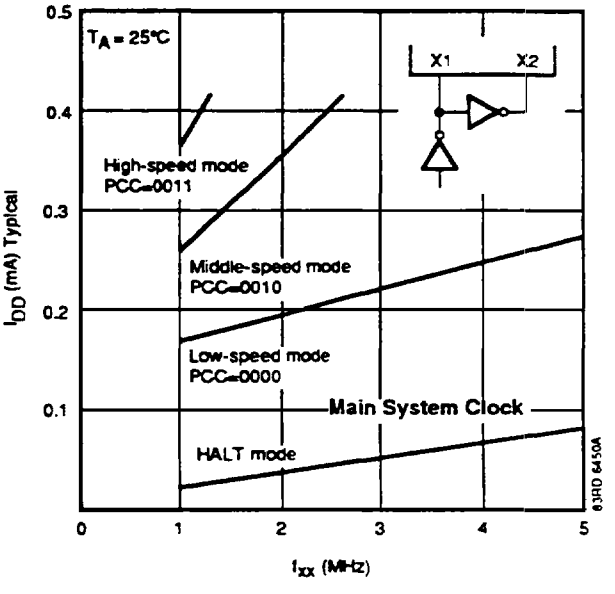


I_{DD} vs f_{XX} (V_{DD} = 5 V)



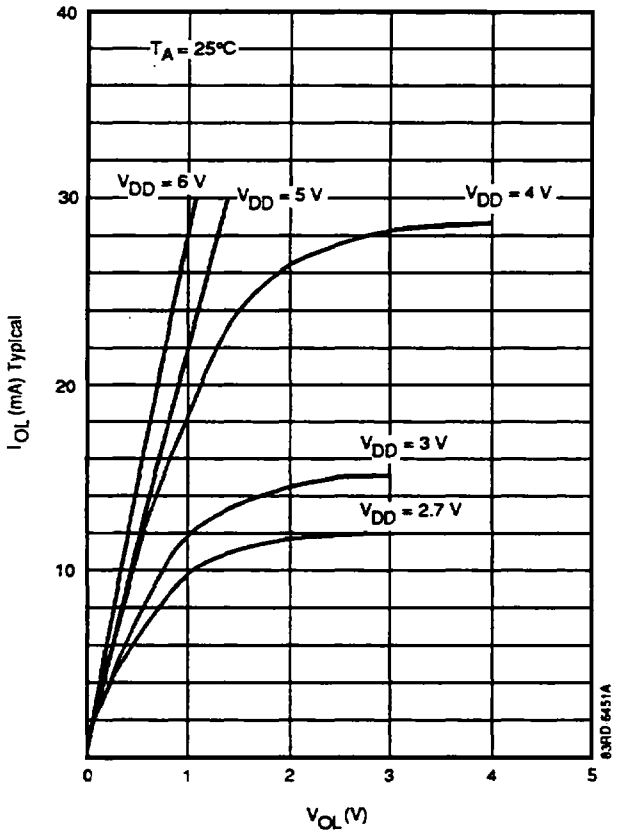


I_{DD} vs f_{XX} (V_{DD} = 3 V)

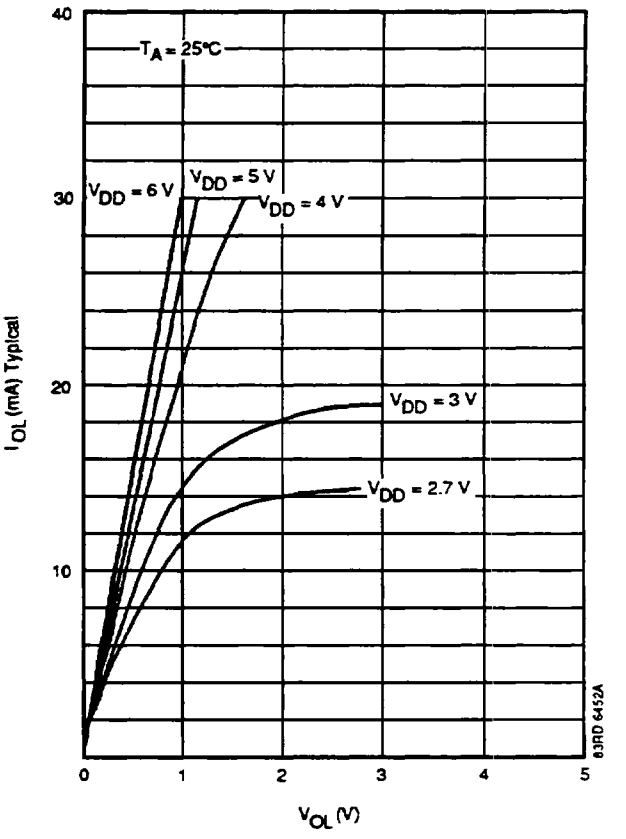


DC Characteristics (cont)

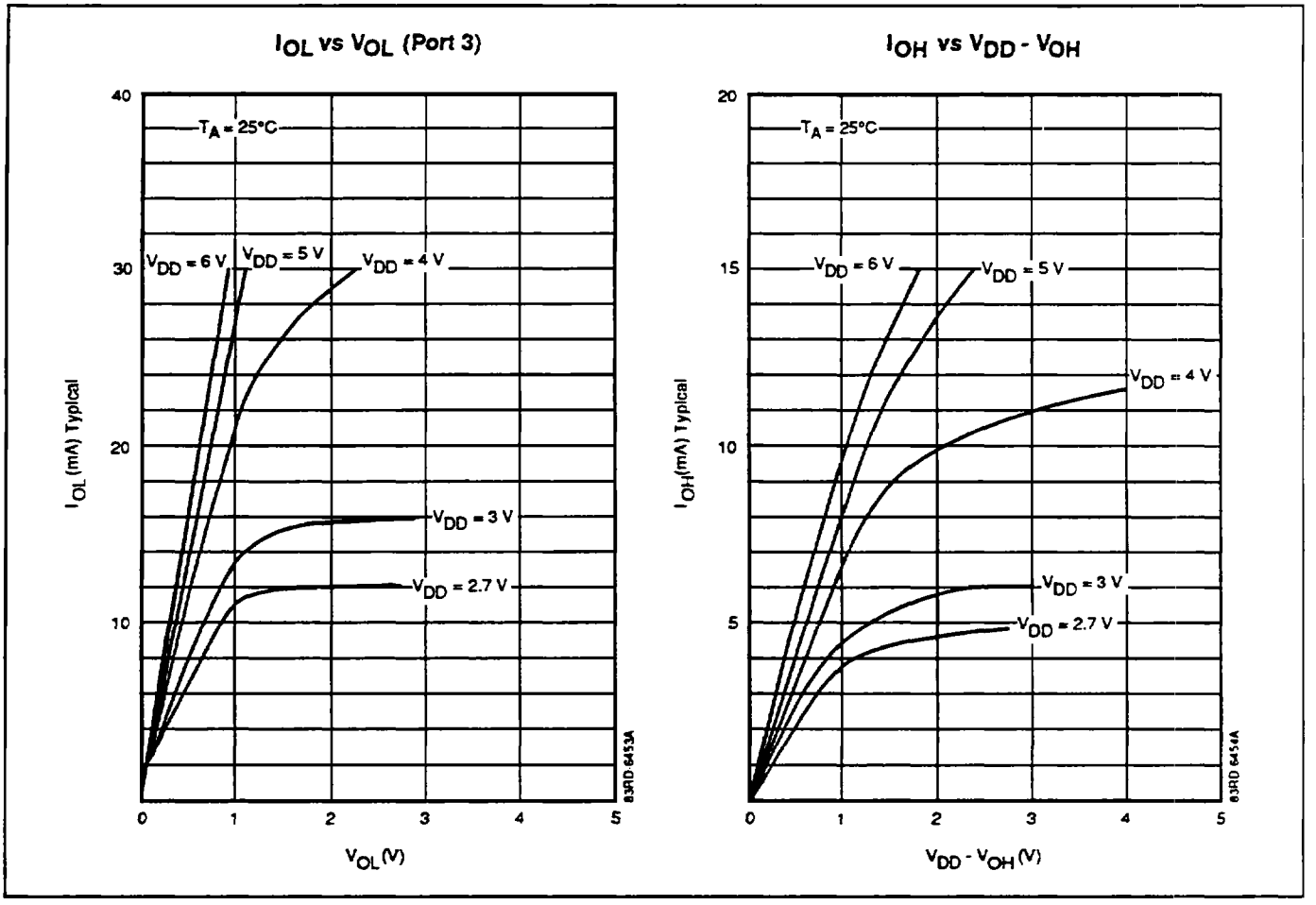
I_{OL} vs V_{OL} (Ports 0, 2, 6, 7)



I_{OL} vs V_{OL} (Ports 4, 5)



DC Characteristics (cont)



AC Characteristics

μPD7500x: T_A = −40 to +85°C, V_{DD} = 2.7 to 6.0 V
μPD75P008: T_A = −10 to +70°C, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Cycle time (Note 1)	t_{CY}	0.95		64	μs	Main system clock (Note 2)
		3.8	(Note 3)	64	μs	Main system clock; V_{DD} = 2.7 to 6.0 V
		114	122	125	μs	Subsystem clock
TI0 input frequency	f_{TI}	0		1	MHz	(Note 2)
		0	(Note 3)	275	kHz	V_{DD} = 2.7 to 6.0 V
TI0 input low- and high-level width	t_{IH}, t_{IL}	0.48			μs	(Note 2)
		1.8	(Note 3)		μs	V_{DD} = 2.7 to 6.0 V
Interrupt inputs low- and high-level width	t_{INTH}, t_{INTL}	(Note 4)			μs	INT0
		10			μs	INT1, INT2, INT4
		10			μs	KR0-KR7
$\overline{\text{RESET}}$ low-level width	t_{RSL}	10			μs	

Notes:

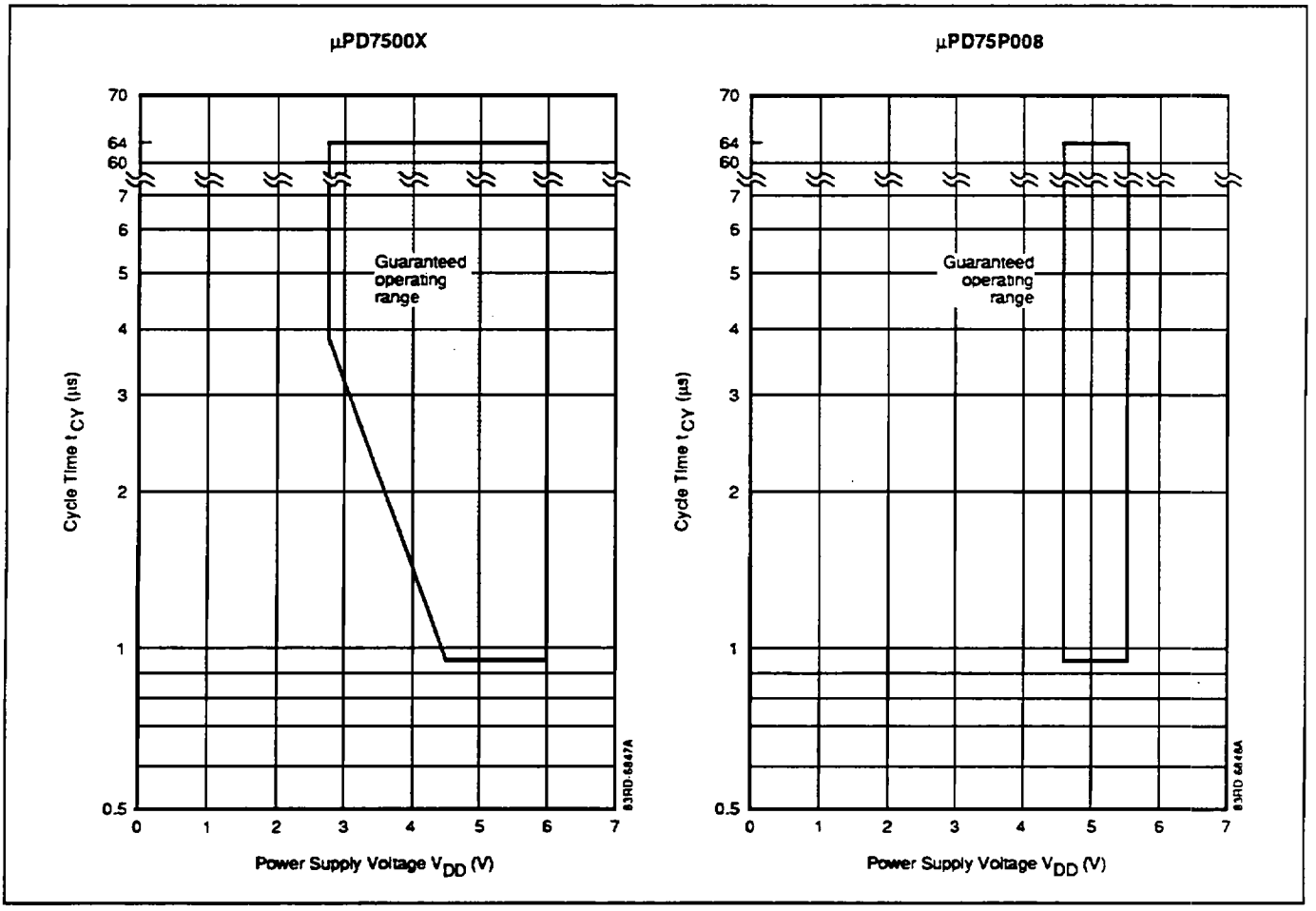
(1) Cycle time (minimum instruction execution time) is determined by the frequency of the oscillator connected to the microcomputer, system clock control register (SCC), and the processor clock control (PCC).

(2) V_{DD} = 4.5 to 6.0 V for 7500x and V_{DD} = 4.5 to 5.5 V for 75P008.

(3) For 7500x only.

(4) $2t_{CY}$ or 128/fx, depending on the setting of the interrupt mode register (IM0).

Figure 3. Guaranteed Operating Range



Serial Transfer Operation

2-line/3-line Serial I/O mode ($\overline{SCK}$..internal clock output)
μPD7500x: T_A = −40 to +85°C, V_{DD} = 2.7 to 6.0 V
μPD75P008: T_A = −10 to +70°C, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
$\overline{SCK}$ cycle time	t_{KCY1}	1600			ns	(Note 1)
		3800	(Note 2)		ns	V_{DD} = 2.7 to 6.0 V
$\overline{SCK}$ low- and high-level width	t_{KL1}, t_{KH1}	$0.5t_{KCY}-50$			ns	(Note 1)
		$0.5t_{KCY}-150$	(Note 2)		ns	V_{DD} = 2.7 to 6.0 V
SI vs. $\overline{SCK}$ ↑ setup time	t_{SIK1}	150			ns	
SI vs. $\overline{SCK}$ ↑ hold time	t_{KSI1}	400			ns	
$\overline{SCK}$ ↓ → SO output delay time (Note 3)	t_{KSO1}			250	ns	(Note 1)
			(Note 2)	1000	ns	V_{DD} = 2.7 to 6.0 V

Serial Transfer Operation

2-line/3-line Serial I/O mode ($\overline{SCK}$..external clock output)
μPD7500x: T_A = −40 to +85°C, V_{DD} = 2.7 to 6.0 V
μPD75P008: T_A = −10 to +70°C, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
$\overline{SCK}$ cycle time	t_{KCY2}	800			ns	(Note 1)
		3200	(Note 2)		ns	V_{DD} = 2.7 to 6.0 V
$\overline{SCK}$ low- and high-level width	t_{KL2}, t_{KH2}	400			ns	(Note 1)
		1600	(Note 2)		ns	V_{DD} = 2.7 to 6.0 V
SI vs. $\overline{SCK}$ ↑ setup time	t_{SIK2}	100			ns	
SI vs. $\overline{SCK}$ ↑ hold time	t_{KSI2}	400			ns	
$\overline{SCK}$ ↓ → SO output delay time (Note 3)	t_{KSO2}			300	ns	(Note 1)
			(Note 2)	1000	ns	V_{DD} = 2.7 to 6.0 V

Notes:

(1) V_{DD} = 4.5 to 6.0 V for 7500x and V_{DD} = 4.5 to 5.5 V for 75P008.

(2) For 7500x only.

(3) The rising edge of the output delay time must be less than 600 ns. For example, if SB0 and SB1 are pulled up with 5 kΩ resistors, the total capacitance of the serial bus line must be no greater than 120 pF.

SBI Mode

$\overline{SCK}$...internal clock output (master)
μPD7500x: T_A = −40 to +85°C, V_{DD} = 2.7 to 6.0 V
μPD75P008: T_A = −10 to +70°C, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
$\overline{SCK}$ cycle time	t_{KCY3}	1600			ns	(Note 1)
		3800	(Note 2)		ns	V_{DD} = 2.7 to 6.0 V
$\overline{SCK}$ low- and high-level width	t_{KL3}, t_{KH3}	$0.5t_{KCY3}-50$			ns	(Note 1)
		$0.5t_{KCY3}-150$	(Note 2)		ns	V_{DD} = 2.7 to 6.0 V
SB0, SB1 vs. $\overline{SCK}$ ↑ setup time	t_{SIK3}	150			ns	
SB0, SB1 vs. $\overline{SCK}$ ↑ hold time	t_{KSI3}	$0.5t_{KCY3}$			ns	
$\overline{SCK}$ ↓ → SB0, SB1 output delay time	t_{KSO3}	0		250	ns	(Note 1)
		0	(Note 2)	1000	ns	V_{DD} = 2.7 to 6.0 V
$\overline{SCK}$ ↑ → SB0, SB1 ↓	t_{KSB}	t_{KCY3}			ns	
SB0, SB1 ↓ → $\overline{SCK}$ ↓	t_{SBK}	t_{KCY3}			ns	
SB0, SB1 low-level width	t_{SBL}	t_{KCY3}			ns	
SB0, SB1 high-level width	t_{SBH}	t_{KCY3}			ns	

SBI Mode

$\overline{SCK}$...external clock output (slave)
μPD7500x: T_A = −40 to +85°C, V_{DD} = 2.7 to 6.0 V
μPD75P008: T_A = −10 to +70°C, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
$\overline{SCK}$ cycle time	t_{KCY4}	800			ns	(Note 1)
		3200	(Note 2)		ns	V_{DD} = 2.7 to 6.0 V
$\overline{SCK}$ low and high level width	t_{KL4}, t_{KH4}	400			ns	(Note 1)
		1600	(Note 2)		ns	V_{DD} = 2.7 to 6.0 V
SB0, SB1 vs. $\overline{SCK}$ ↑ setup time	t_{SIK4}	100			ns	
SB0, SB1 vs. $\overline{SCK}$ ↑ hold time	t_{KSI4}	$0.5t_{KCY4}$			ns	
$\overline{SCK}$ ↓ → SB0, SB1 output delay time	t_{KSO4}	0		300	ns	(Note 1)
		0	(Note 2)	1000	ns	V_{DD} = 2.7 to 6.0 V
$\overline{SCK}$ ↑ → SB0, SB1 ↓	t_{KSB}	t_{KCY4}			ns	
SB0, SB1 ↓ → $\overline{SCK}$ ↓	t_{SBK}	t_{KCY4}			ns	
SB0, SB1 low-level width	t_{SBL}	t_{KCY4}			ns	
SB0, SB1 high-level width	t_{SBH}	t_{KCY4}			ns	

Notes:

(1) V_{DD} = 4.5 to 6.0 V for 7500x and V_{DD} = 4.5 to 5.5 V for 75P008.

(2) For 7500x only.

Data Memory STOP Mode Low Voltage Data Retention Characteristics

μPD7500x: T_A = −40 to +85°C
μPD75P008: T_A = −10 to +70°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Data retention voltage	V_{DDDR}	2.0		(Note 1)	V	
Data retention current (Note 2)	I_{DDDR}		0.1	10	μA	V_{DDDR} = 2.0 V
Release signal SET time	t_{SREL}	0			μs	
Oscillation stabilization time (Note 3)	t_{WAIT}		$2^{17}/f_{XX}$		s	Release by $\overline{RESET}$ input
			(Note 3)		ms	Release by interrupt request

Notes:

(1) Max = 6.0 V for 7500x and 5.5 V for 75P008.

(2) Pull-up resistor current, comparator circuit current, and power-on-reset current is not included in this table.

(3) Oscillation stabilization WAIT time is the time during which the CPU is stopped to prevent unstable operation when the oscillation is started. WAIT time depends on the resonator vendor's specifications. The wait time generated by the chip should be ≧ vendor's spec and the setting of the basic interval timer mode register (BTM) according to the following table:

BTM3	BTM2	BTM1	BTM0	WAIT time (f_{XX} = 4.19 MHz)
–	0	0	0	$2^{20}/f_{XX}$ (approx 250 ms)
–	0	1	1	$2^{17}/f_{XX}$ (approx 31.3 ms)
–	1	0	1	$2^{15}/f_{XX}$ (approx 7.82 ms)
–	1	1	1	$2^{13}/f_{XX}$ (approx 1.95 ms)

DC Programming Characteristics (For 75P008 only)

T_A = 25 ±5°C; V_{DD} = 6.0 ±0.25 V; V_{PP} = 12.5 ±0.3 V; V_{SS} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
High-level input voltage	V_{IH1}	$0.7V_{DD}$		V_{DD}	V	All except X1, X2
	V_{IH2}	V_{DD}−0.5		V_{DD}	V	X1, X2
Low-level input voltage	V_{IL1}	0		$0.3V_{DD}$	V	All except X1, X2
	V_{IL2}	0		0.4	V	X1, X2
Input leakage current	I_{LI}			10	μA	V_{IN} = V_{IL} or V_{IH}
High-level output voltage	V_{OH}	V_{DD}−1.0			V	I_{OH} = −1 mA
Low-level output voltage	V_{OL}			0.4	V	I_{OL} = 1.6 mA
V_{DD} supply current	I_{DD}			30	mA	
V_{PP} supply current	I_{PP}			30	mA	MD0 = V_{IL}; MD1 = V_{IH}

Notes:

(1) V_{PP} must not exceed +13.5 V, including over shoot.

(2) V_{DD} must be applied before V_{PP} and is turned off after V_{PP} is removed.

AC Programming Characteristics (For 75P008 only)

T_A = 25 ± 5°C; V_{DD} = 6.0 ± 0.25 V; V_{PP} = 12.5 ± 0.3 V; V_{SS} = 0 V

Parameter	Symbol	(Note 1)	Min	Max	Unit	Conditions
Address setup time (Note 2)	t_{AS}	t_{AS}	2		μs	
MD1 to MD0 ↓ setup	t_{M1S}	t_{OES}	2		μs	
Data to MD0 ↓ setup	t_{DS}	t_{DS}	2		μs	
Address hold from MD0 ↑ (Note 2)	t_{AH}	t_{AH}	2		μs	
Data hold from MD0 ↑	t_{DH}	t_{DH}	2		μs	
Data output float delay from MD0 ↑	t_{DF}	t_{DF}	0	130	ns	
V_{PP} setup to MD3 ↑	t_{VPS}	t_{VPS}	2		μs	
V_{DD} setup to MD3 ↑	t_{VDS}	t_{VCS}	2		μs	
Initialized program pulse width	t_{PW}	t_{PW}	0.95	1.05	ms	
Additional program pulse width	t_{OPW}	t_{OPW}	0.95	21	ms	
MD0 setup to MD1 ↑	t_{MOS}	t_{CES}	2		μs	
Data output delay from MD0 ↓	t_{DV}	t_{DV}		1	μs	MD0 = MD1 = V_{IL}
MD1 hold to MD0 ↑	t_{M1H}	t_{OEH}	2		μs	$t_{M1H} + t_{M1R} \geq 50$ μs
MD1 recovery from MD0 ↓	t_{M1R}	t_{OR}	2		μs	$t_{M1H} + t_{M1R} \geq 50$ μs
Program counter reset	t_{PCR}		10		μs	
X1 input low- and high-level width	t_{XH}, t_{XL}		0.125		μs	
X1 input frequency	f_X			4.19	MHz	
Initial mode set	t_I		2		μs	
MD3 setup to MD1 ↑	t_{M3S}		2		μs	
MD3 hold from MD1 ↓	t_{M3H}		2		μs	
MD3 setup to MD0 ↓	t_{M3SR}		2		μs	During program read cycle
Data delay from address (Note 2)	t_{DAD}	t_{ACC}	2		μs	
Data output hold from address (Note 2)	t_{HAD}	t_{OH}	0	130	ns	
MD3 output hold from MD0 ↑	t_{M3HR}		2		μs	
Data output float delay from MD3 ↓	t_{DFR}		2		μs	

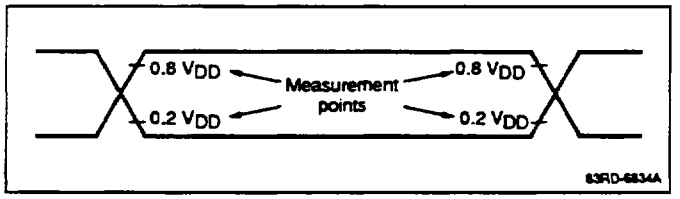
Notes:

(1) These symbols correspond to those of the μPD27C256 EPROM.

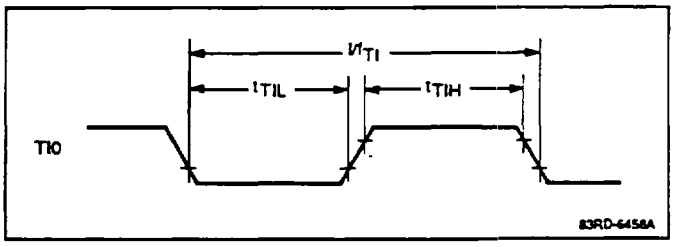
(2) The internal address signal is incremented by the rising edge of the fourth X1 pulse; it is not connected to an external pin.

Timing Waveforms

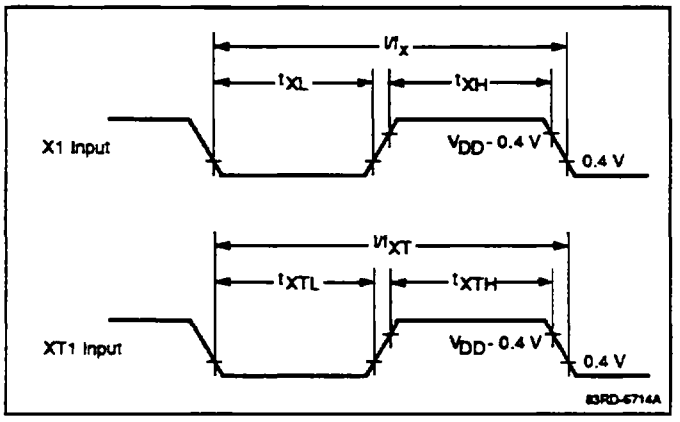
AC Timing Measurements Points (Except X1 and XT1)



TI0 Timing

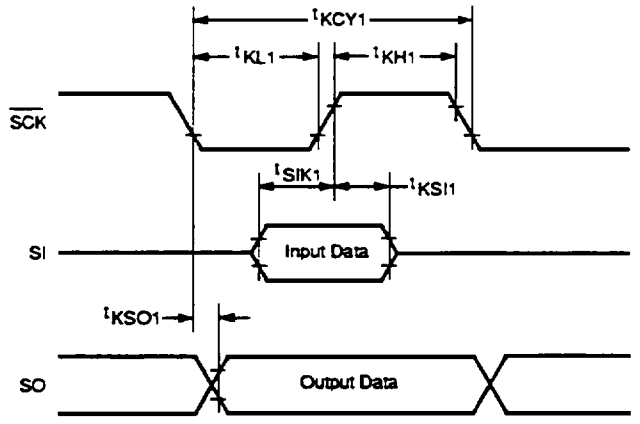


Clock Timing

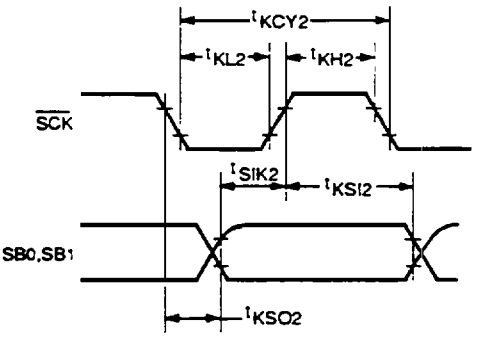


Serial Transfer Timing

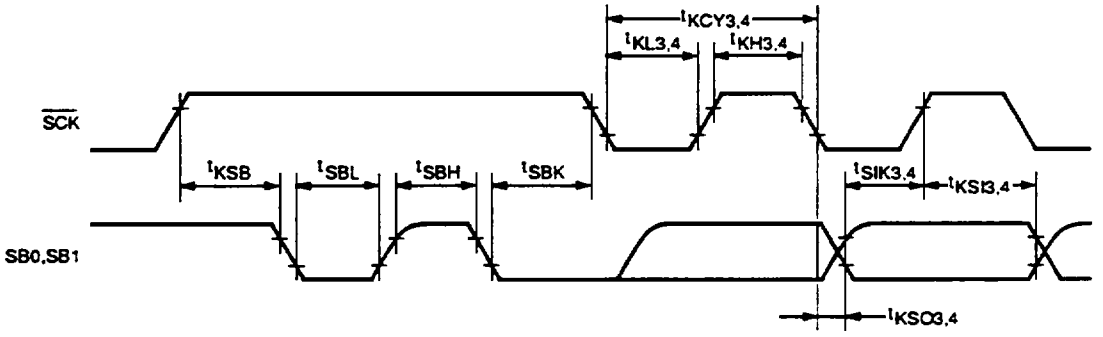
Serial I/O Mode (3-Line)



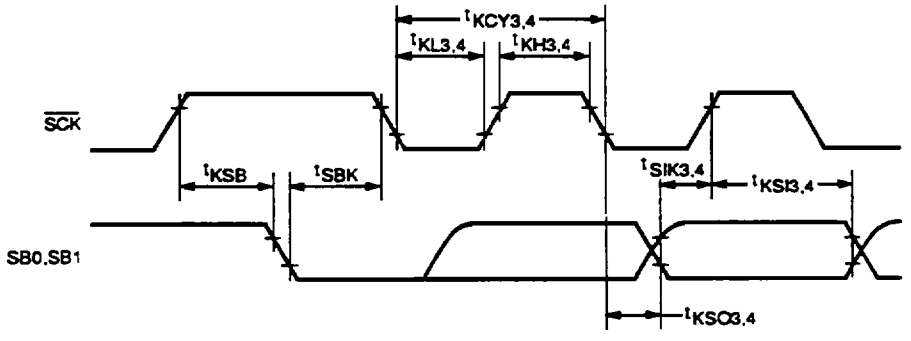
Serial I/O Mode (2-Line)



SBI Mode Bus Release Signal Transfer Timing



SBI Mode Command Signal Transfer Timing



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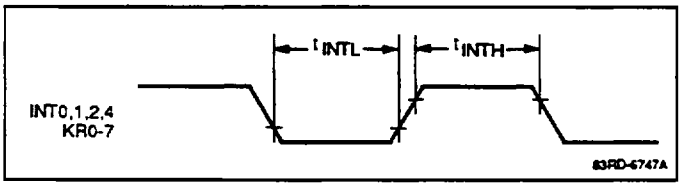
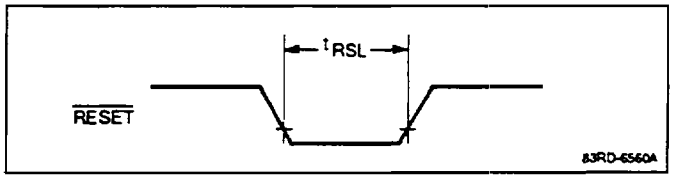
Interrupt Input Timing

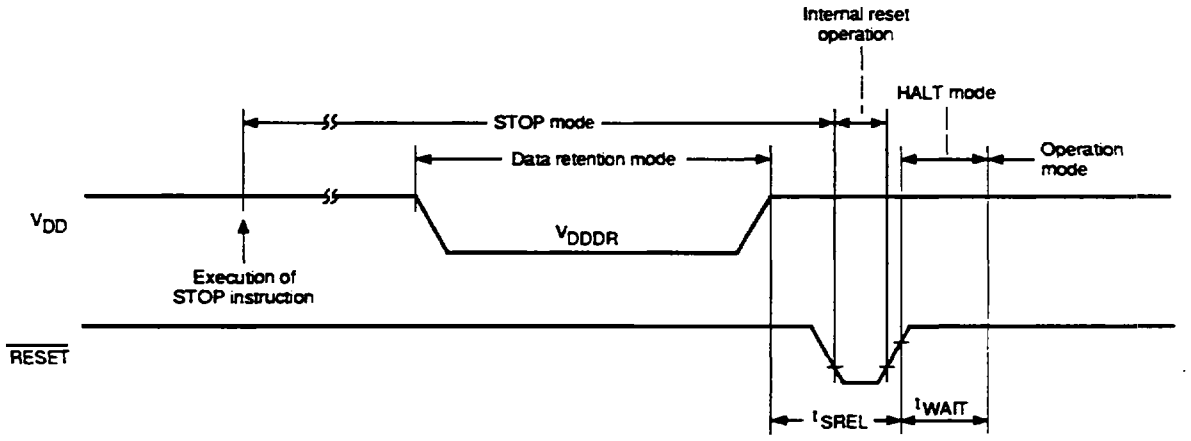


RESET Input Timing

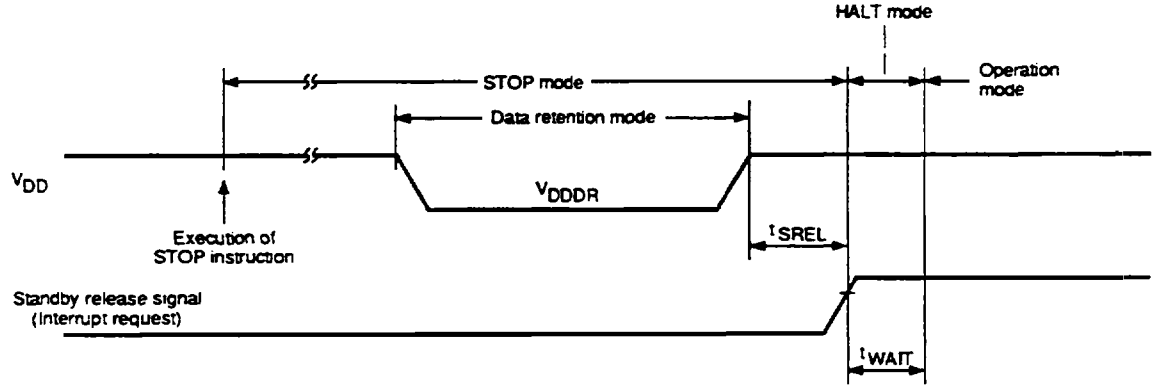


Data Retention Timing

A. STOP mode is released by RESET input

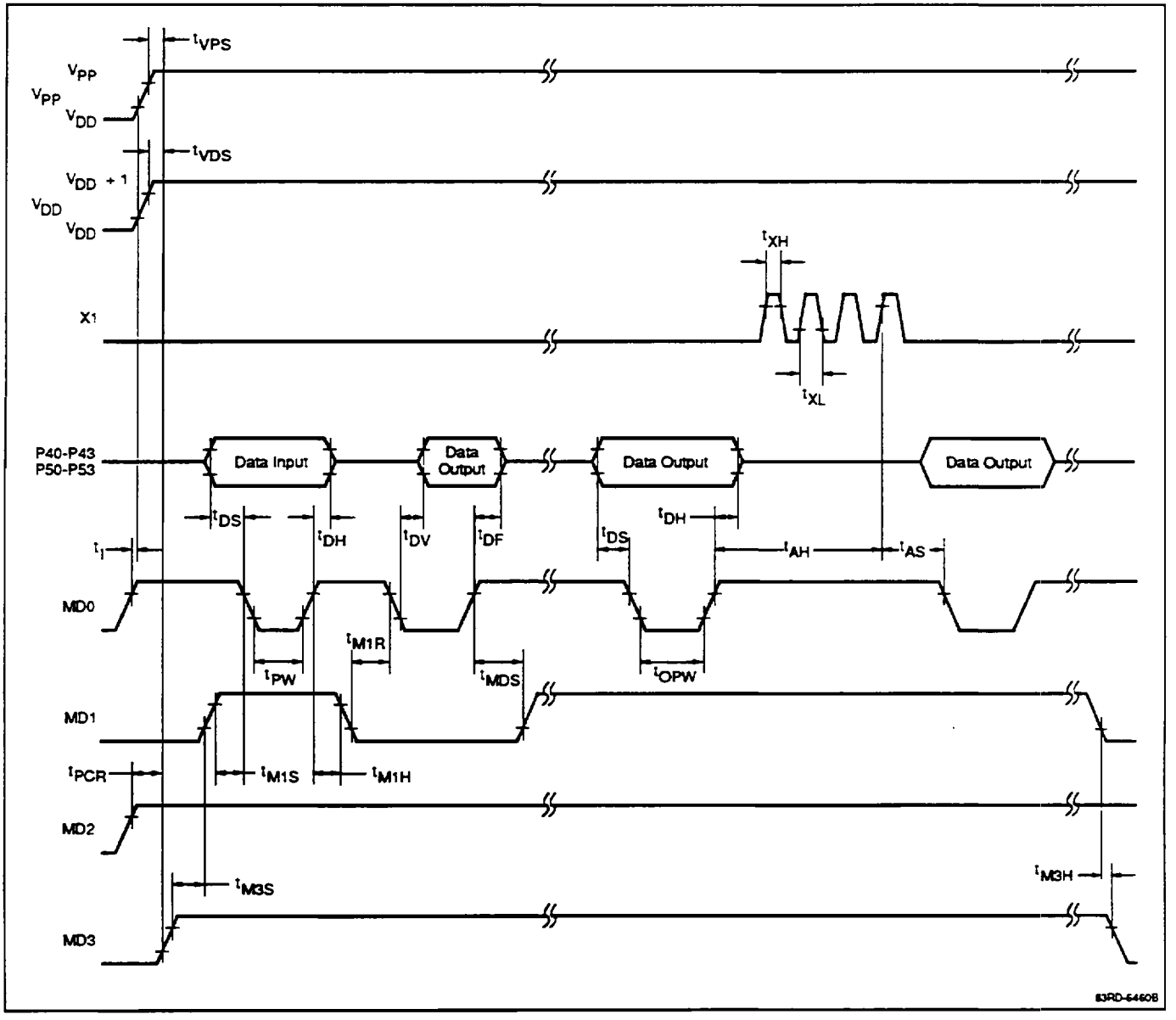


B. STOP mode is released by interrupt signal



83RD-6456B

Program Memory Write/Verify Timing (μPD75P008)



Program Memory Read Timing (μPD75P008)